CLAIMS

What is claimed is:

1. A method for providing a connection between a source endpoint and a destination endpoint through a fibre channel switch, the method comprising:

receiving FICON frames at the ingress port of a fibre channel switch from a source endpoint, each frame having a header that includes FICON address information;

mapping the FICON address information of each received FICON frame to internal address information at the ingress port to provide internal frames;

switching the internal frames through the fibre channel switch to an egress port according to the internal address information; and

mapping the internal address information of each internal frame to the FICON address information at the egress port for transmission to the destination endpoint.

2. The method of Claim 1 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein mapping the FICON address information includes mapping the FICON destination address to an internal destination address.

3. The method of Claim 2 wherein the FICON destination address includes an 8 bit domain field, an 8 bit port field and an 8 bit loop field and wherein the internal destination address includes a 4 bit fabric field, a 6 bit chassis field, a 2 bit switch field, a 2 bit internal port field and an 8 bit internal loop field.

4. The method of Claim 3 wherein mapping the FICON destination address to the internal destination address includes mapping the four most significant bits of the domain field to the 4 bit fabric field, mapping the least significant bit of the domain field and the five most significant bits of the port field to the 6 bit chassis field, mapping the three least significant bits of the port field to the 2 bit switch field and the most significant bit of the internal port field, setting the least significant bit of the internal port field to 0 for even addressing or to 1 for odd addressing, and mapping the 8 bit loop field to the 8 bit internal loop field.

5. The method of Claim 3 wherein mapping the internal destination address to the FICON destination address includes mapping an 8 bit domain address from a domain address register to the 8 bit domain field, mapping the five least significant bits of the chassis field to the five most significant bits of the 8 bit port field, mapping the 2 bit switch field and the most significant bit of the internal port field to the three least significant bits of the 8 bit port field, and mapping the 8 bit internal loop field to the 8 bit loop field.

6. The method of Claim 1 wherein the fibre channel switch is one of a plurality of fibre channel switches of a fibre channel switch fabric and further comprising preassigning a chassis address to the fibre channel switch, each chassis having a specific switch address that is different from the preassigned chassis address.

7. The method of Claim 6 further comprising providing in the fibre channel switch a chassis size register to indicate the overall number of ports in the switch fabric, a chassis address match register that includes a logical chassis address, and a reserved chassis address register that includes a physical chassis address of switches within the switch fabric.

8. The method of Claim 7 wherein the FICON address information includes a destination D_ID and mapping the FICON address information includes comparing the chassis address bits of the destination D_ID with the chassis address match register and, upon a match, concatenating a portion of the port address in the D_ID with the reserved chassis address from the reserved chassis address register to provide an internal chassis address of the switch within the fabric.

9. The method of Claim 8 wherein mapping the internal address information includes comparing the internal chassis address against the reserved address register and inserting the contents of the chassis address register into the destination D_ID.

10. The method of Claim 7 wherein the reserved chassis address includes 8 addresses and the chassis size register indicates 64 ports.

11. The method of Claim 7 wherein the reserved chassis address includes 16 addresses and the chassis size register indicates 128 ports.

12. The method of Claim 7 wherein the reserved chassis address includes 32 addresses and the chassis size register indicates 256 ports.

13. The method of Claim 7 wherein the FICON address information includes a destination D_ID and mapping the FICON address information includes mapping a logical port address in the destination D_ID to a spared port address from a lookup table.

14. The method of Claim 1 wherein the FICON frame includes a cyclic redundancy check (CRC) and wherein mapping the FICON address information to internal address information includes recalculating the CRC and inserting the recalculated CRC into the internal frame.

15. The method of Claim 14 wherein mapping the internal address information to FICON address information includes recalculating the CRC and inserting the recalculated CRC into the FICON frame at the egress port.

16. A switch for providing a connection between a source endpoint and a destination endpoint, the switch comprising:

an ingress port for receiving inbound FICON frames from a source endpoint, each frame having a header that includes FICON address information;

an address adaptor for mapping the FICON address information of each received FICON frame to internal address information to provide internal frames; and

a switch element for switching the internal frames according to the internal address information.

17. The switch of Claim 16 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein the address adaptor is operable to map the FICON destination address to an internal destination address.

18. The switch of Claim 17 wherein the FICON destination address includes an 8 bit domain field, an 8 bit port field and an 8 bit loop field and wherein the internal destination address includes a 4 bit fabric field, a 6 bit chassis field, a 2 bit switch field, a 2 bit internal port field and an 8 bit internal loop field.

19. The switch of Claim 18 wherein the address adaptor is operable to map the FICON destination address to the internal destination address by mapping the four most significant bits of the domain field to the 4 bit fabric field, mapping the least significant bit of the domain field and the five most significant bits of the port field to the 6 bit chassis field, mapping the three least significant bits of the port field to the 2 bit switch field and the most significant bit of the internal port field, setting the least significant bit of the internal port field to 0 for even addressing or to 1 for odd addressing, and mapping the 8 bit loop field to the 8 bit internal loop field.

20. The switch of Claim 16 further comprising a second address adaptor for mapping the internal address information of each internal frame to the FICON address information to provide outbound FICON frames and an egress port for transmitting the outbound FICON frames to a destination endpoint.

21. The switch of Claim 20 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein the second address adaptor is operable to map the internal destination address to a FICON destination address.

22. The switch of Claim 21 wherein the second address adaptor is operable to map the internal destination address to the FICON destination address by mapping an 8 bit domain address from a domain address register to the 8 bit domain field, mapping the five least significant bits of the chassis field to the five most significant bits of the 8 bit port field, mapping the 2 bit switch field and the most significant bit of the internal port field to the three least significant bits of the 8 bit port field, and mapping the 8 bit internal loop field to the 8 bit loop field.

23. The switch of Claim 16 wherein the switch is one of a plurality of fibre channel switches of a fibre channel switch fabric and wherein a chassis address is preassigned to the fibre channel switch, each chassis having a specific switch address that is different from the preassigned chassis address.

24. The switch of Claim 23 wherein the address adaptor further comprises a chassis size register to indicate the overall number of ports in the switch fabric, a chassis address match register that includes a logical chassis address, and a reserved chassis address register that includes a physical chassis address of the switch.

25. The switch of Claim 24 wherein the FICON address information includes a destination D_ID and wherein the address adaptor is operable to map the FICON address information by comparing the chassis address bits of the destination D_ID with the chassis address match register and, upon a match, concatenating a portion of the port address in the D_ID with the reserved chassis address from the reserved chassis address register to provide an internal chassis address of the switch within the fabric.

26. The switch of Claim 25 wherein the reserved chassis address includes 8 addresses and the chassis size register indicates 64 ports.

27. The switch of Claim 25 wherein the reserved chassis address includes 16 addresses and the chassis size register indicates 128 ports.

28. The switch of Claim 25 wherein the reserved chassis address includes 32 addresses and the chassis size register indicates 256 ports.

29. The switch of Claim 16 wherein the FICON address information includes a destination D_ID and wherein the address adaptor is operable to map a logical port address in the destination D_ID to a spared port address from a lookup table.

30. The switch of Claim 16 wherein the FICON frame includes a cyclic redundancy check (CRC) and wherein the address adaptor is operable to recalculate the CRC and insert the recalculated CRC into the internal frame.

31. In a fibre channel switch, an address adaptor comprising:

an inbound frame processor for receiving inbound frames from a source endpoint, each inbound frame having a header that includes first address information having a first format, the inbound frame processor including address logic for mapping the first address information of each received inbound frame to second address information having a second format to provide inbound internal frames to a switch fabric; and

an outbound frame processor for receiving outbound internal frames from a switch fabric, the outbound frame processor including address logic for mapping the second address information of each outbound internal frame to first address information having the first format to provide outbound frames for transmission to a destination endpoint.

32. The address adaptor of Claim 31 wherein the first format has continuous addressing and the second format has discontinuous addressing.

33. The address adaptor of Claim 31 wherein the first format is FICON format and the second format is an internal format.

34. The address adaptor of Claim 33 wherein the FICON address information comprises a FICON destination address and the internal address information includes an internal destination address and wherein the address adaptor is operable to map between a FICON destination address to an internal destination address.

35. The address adaptor of Claim 34 wherein the FICON destination address includes an 8 bit domain field, an 8 bit port field and an 8 bit loop field and wherein the internal destination address includes a 4 bit fabric field, a 6 bit chassis field, a 2 bit switch field, a 2 bit internal port field and an 8 bit internal loop field and wherein the address adaptor is operable to map the FICON destination address to the internal destination address by mapping the four most significant bits of the domain field to the 4 bit fabric field, mapping the least significant bit of the domain field and the five most significant bits of the port field to the 6 bit chassis field, mapping the three least significant bits of the port field to the 2 bit switch field and the most significant bit of the internal port field, setting the least significant bit of the internal port field to 0 for even addressing or to 1 for odd addressing, and mapping the 8 bit loop field to the 8 bit internal loop field.

36. The address adaptor of Claim 35 wherein the address adaptor is operable to map the internal destination address to the FICON destination address by mapping an 8 bit domain address from a domain address register to the 8 bit domain field, mapping the five least significant bits of the chassis field to the five most significant bits of the 8 bit port field, mapping the 2 bit switch field and the most significant bit of the internal port field to the three least significant bits of the 8 bit port field, and mapping the 8 bit internal loop field to the 8 bit loop field.

37. The address adaptor of Claim 31 for use in a fibre channel switch fabric comprising at least one switch and at least one chassis, wherein all or a portion of the switches in the fabric are preassigned a chassis address, and each chassis has a specific switch address that is different from the preassigned chassis address.

38. The address adaptor of Claim 37 wherein the address logic of the inbound frame processor includes a chassis size register to indicate the overall number of ports in the switch fabric, a chassis address match register that includes a logical chassis address, and a reserved address register that includes a physical chassis address of switches within the switch fabric.

39. The address adaptor of Claim 38 wherein the FICON address information includes a destination D_ID and the address logic is operable to map the FICON address information by comparing the chassis address bits of the destination D_ID with the chassis address match register and, upon a match, concatenating a portion of the port address in the D_ID with the reserved chassis address from the reserved chassis address register to provide an internal chassis address of the switch within the fabric.

40. The address adaptor of Claim 39 wherein the reserved chassis address includes 8 addresses and the chassis size register indicates 64 ports.

41. The address adaptor of Claim 39 wherein the reserved chassis address includes 16 addresses and the chassis size register indicates 128 ports.

42. The address adaptor of Claim 39 wherein the reserved chassis address includes 32 addresses and the chassis size register indicates 256 ports.

43. The address adaptor of Claim 37 wherein the FICON address information includes a destination D_ID and wherein the address adaptor is operable to map a logical port address in the destination D_ID to a spared port address from a lookup table.

44. The address adaptor of Claim 31 wherein the inbound frame includes a cyclic redundancy check (CRC) and wherein the inbound frame processor is operable to recalculate the CRC and insert the recalculated CRC into the inbound internal frame.

45. The address adaptor of Claim 44 wherein the outbound frame processor is operable to recalculate the CRC and insert the recalculated CRC into the outbound frame.

46. A switch for providing a connection between a source endpoint and a destination endpoint, the switch comprising:

means for receiving FICON frames from a source endpoint, each frame having a header that includes a FICON destination address;

means for mapping the FICON destination address of each received FICON frame to an internal destination address to provide internal frames;

means for switching the internal frames through the switch according to the internal destination address; and

means for mapping the internal destination address of each internal frame to the FICON destination address for transmission to the destination endpoint.

47. In an input/output port of a switch, a method of buffer management comprising:

providing a switch element that includes a first buffer;

providing a second buffer;

monitoring the buffer level of the first buffer and the second buffer;

upon receipt of a data frame, checking the buffer levels of the first and second buffers;

writing the received data frame to the second buffer if the first buffer is full; otherwise, passing the received data frame to the first buffer if the first buffer is not full and the second buffer is empty; otherwise, reading a data frame from the second buffer and passing the read data frame to the first buffer if the first buffer is not full and the second buffer in not empty.

48. The method of Claim 47 wherein the second buffer is larger than the first buffer.

49. The method of Claim 47 further comprising detecting a start of frame (SOF) in data frames sent to the first buffer, detecting a buffer ready (RDY) signal sent from the switch element upon emptying a data frame from the first buffer, incrementing a first buffer counter upon detection of SOF and decrementing the first buffer counter upon detection of RDY.

50. The method of Claim 47 further comprising detecting a start of frame (SOF) in data frames written to the second buffer, detecting an end of frame (EOF) in data frames read from the second buffer, incrementing a second buffer counter upon detection of SOF and decrementing the second buffer counter upon detection of EOF.

51. A switch comprising:

at least one ingress port for receiving data frames from a source endpoint;

a switch element for switching the data frames, the switch element having a first buffer;

an adaptor coupled between the ingress port and the switch element and having a second buffer and a buffer controller for monitoring the buffer level of the first buffer and the second buffer wherein upon receipt of a data frame, the buffer controller is operable to check the buffer levels of the first and second buffers and to write the received data frame to the second buffer if the first buffer is full; otherwise, to pass the received data frame to the first buffer if the first buffer is not full and the second buffer is empty; otherwise, to read a data frame from the second buffer and pass the read data frame to the first buffer if the first buffer is not full and the second buffer in not empty.

52. The switch of Claim 51 wherein the second buffer is larger than the first buffer.

53. The switch of Claim 51 wherein the adaptor further includes first buffer logic comprising a first detector for detecting a start of frame (SOF) in data frames sent to the first buffer, a second detector for detecting a buffer ready (RDY) signal sent from the switch element upon emptying a data frame from the first buffer, and a first buffer counter incremented upon detection of SOF and decremented upon detection of RDY.

54. The switch of Claim 51 wherein the adaptor further includes second buffer logic comprising a first detector for detecting a start of frame (SOF) in data frames written to the second buffer, a second detector for detecting an end of frame (EOF) in data frames read from the second buffer, and a second buffer counter incremented upon detection of SOF and decremented upon detection of EOF.

55. A method for providing a connection between a source endpoint and a destination endpoint through a data switch, the method comprising:

receiving inbound frames at the ingress port of the data switch from a source endpoint, each frame having a header that includes first destination address information;

mapping the first destination address information of each received frame to internal destination address information at the ingress port to provide internal frames;

switching the internal frames through the data switch to an egress port according to the internal destination address information; and

mapping the internal destination address information of each internal frame to the first destination address information at the egress port for transmission to the destination endpoint.

56. A switch for providing a connection between a source endpoint and a destination endpoint, the switch comprising:

an ingress port for receiving inbound frames from a source endpoint, each frame having a header that includes first destination address information;

an address adaptor for mapping the first destination address information of each received frame to internal address information to provide internal frames; and

a switch element for switching the internal frames according to the internal address information.

57. A method for providing a connection between a source endpoint and a destination endpoint through a network of data switches, the method comprising:

receiving inbound frames at the ingress port of a first data switch in the network from a source endpoint, each frame having a header that includes first destination address information;

mapping the first destination address information of each received frame to internal destination address information at the ingress port to provide internal frames;

switching the internal frames through the network of data switches to an egress port of a second data switch in the network according to the internal destination address information; and

mapping the internal destination address information of each internal frame to the first destination address information at the egress port for transmission to the destination endpoint.

58. A network of data switches for providing a connection between a source endpoint and a destination endpoint, the network comprising:

at least one ingress port at a first data switch in the network for receiving inbound frames from a source endpoint, each frame having a header that includes first destination address information;

at least one address adaptor at the first data switch for mapping the first destination address information of each received frame to internal address information to provide internal frames;

at least another address adaptor at a second data switch in the network for mapping the internal destination address information of each internal frame to the first destination address information to provide outbound frames; and

at least one egress port at the second data switch for transmitting the outbound frames to a destination point.